REMARKS

This responds to the non-final Office Action mailed on February 06, 2008. Reconsideration is respectfully requested.

Claims 1 – 5, 8, 22 – 26, 28, 30, 32, 34, 35, 47 – 52, 54 – 62 and 64 - 70 are amended, claims 7, 31, 53 and 63 are canceled, and no claims are added; as a result, claims 1 – 6, 8 – 30, 32 – 52, 54 – 62 and 64 - 71 remain pending in this application.

§102 and §103 Rejections of the Claims

Claims 1, 2, 19 – 21, 24 – 27, 70 and 71 were rejected under 35 U.S.C. § 102(e) for anticipation by Naylor et al. (G.B. 2,337,138). Claims 3 – 18, 22, 23, 28 – 62 and 64 – 69 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Naylor et al. (G.B. 2,337,138), in view of Edens (U.S. 6,611,537), and Borland et al (U.S. 6,724,772).

Applicant's claim 1 is directed to an integrated circuit for processing media data that includes a data path arranged in a ring configuration to communicate the media data at different sampling rates synchronized with a sample-locked rate. The integrated circuit includes a plurality of processing modules positioned within the data path to process the media data, a routing controller; and a digital interface. As recited in claim 1, the data path comprises a plurality of separate portions to communicate data between adjacent of the processing modules. The separate portions of the data path couple the adjacent processing modules in series to communicate the media data between the adjacent processing modules. As further recited in claim 1, the routing controller is configured to clock the media data in time-slots between the adjacent processing modules around the separate portions of the data path to provide communications from a source processing module to a target processing module. The number of time-slots available for each of the different sampling rates is inversely related to each different sampling rate. Each processing module is assigned a fixed output time-slot and a variable input time-slot.

As recited in claim 1, the synchronization of the media data with a sample-locked rate (e.g., a master sampling rate) and the use of a different number of time-slots for each different sampling rate allow media data of different sampling rates to be communicated around the data path. The number of the time-slots available for each of the different sample rates is inversely

related to the particular sampling rate. For example, when 4096 total time-slots are provided, the data path may support sample rates of up to 384 KHz by allocating one time-slot for a sample rate of 48 KHz, two time-slots for a sample rate of 96 KHz, four time-slots for a sample rate of 192 KHz, and eight time-slots for the 384 KHz sample rate. The ability to communicate media data at different sampling rates and the communication of media data at different sampling rates using different numbers of time-slots is not taught or suggested by any of the cited references.

As further recited in claim 1, the fixed output time-slot assigned to each processing module may allow each processing module to output data in a same predetermined time-slot without any handshaking and without any additional delay. The variable number of input time-slots may allow a processing module to receive data in one or more different time-slots under control of the routing controller. This is not taught or suggested by any of the cited references.

Naylor has been cited by the Examiner for disclosing, among other things, processing modules in a ring-configuration in which synchronous operation is achieved using a clock edge. Unlike Applicant's claim 1 which recites the use of assigned time-slots, Naylor uses a two-signal handshake to transfer data packets between modules (see Naylor page 6 line 33 through page 7 line 5). This handshake process requires additional processing resources and the time required to perform the two-signal handshake required time, delaying the transfer of data. Furthermore, since Naylor does not use assigned time-slots, data to be transferred can be significantly delayed. For example, in Naylor when the receiving link is busy, when the next link ahead of it is busy, or when the host is inserting a payload, the data is held off as long as required (see Naylor page 7 lines 20 – 23).

Edens has been cited by the Examiner for, among other things, disclosing a time-multiplexing scheme which eliminates the delay disclosed by Naylor. This time-multiplexing scheme in which processing modules are assigned input and output time-slots, however, is incompatible with the bus architecture of Naylor because Naylor transfers data on a per packet basis. Unlike Applicant's claim 1, data from more than one module cannot be present at the same time on Naylor's bus. In Naylor, the bus allocation is varied based on packet size, whether packets are part of a sequence, and based on packet priority. The use of the various buffers in Naylor is designed to specifically accommodate payload variability and efficiently use the bus (see Naylor page 7 line 33 through page 9 line 7). The technique is incompatible with the time-

multiplexing scheme of Edens because Edens requires the use of fixed length frames, and the transmission and reception of information on every clock cycle (see Edens abstract). Therefore, Edens cannot be combined with Naylor.

Edens, furthermore does not teach or suggest the communication of media data at different sampling rates synchronized with a sample-locked rate, as recited in claim 1. Edens also does not teach or suggest that the number of the time-slots available for each of the different sampling rates is inversely related to each different sampling rate, as recited in claim 1. Edens also does not teach or suggest that each processing module is assigned a fixed output time-slot and a variable input time-slot, as recited in claim 1. In Edens, a fixed data rate per frame is used (see Edens column 10 lines 55 – 66 and column 26 lines 26 - 30). To accommodate different bandwidth data streams, the data stream is divided into distinct channels that are simultaneously transmitted (i.e., to maintain phase coherency) (see Edens column 11 lines 5 – 20).

Borland has been cited by the Examiner for disclosing the communication of digital audio data in time-slots of assigned frequency and assigned length. Borland's system is incompatible with a ring-configuration because Borland uses a single bus 330 accessible and shared by all modules 210A – 210H. Borland also reassigns time-slots based on priority (see Borland column 6 lines 16 – 24) rather than assigning a fixed output time-slot and a variable input time-slot to each processing module, as recited in Applicant's claim 1. Assigning a fixed output time-slot and a variable input time-slot to each processing module would be highly inefficient on Borland's shared bus. Therefore, Applicant submits that there would be no reason to combine Borland with any of the other cited references.

In view of the above, Applicant submits that claim 1 is allowable over the cited references and that the rejection of claim 1 has been overcome. Claims 22, 24 and 47 have recitations similar to claim 1 and are also believed to be allowable. Claims 2 – 6, 8 – 21 and 70 – 71 are believed to be allowable at least because of their dependency on claim 1. Claim 23 is believed to be allowable at least because of their dependency on claim 22. Claims 25 – 30 and 32 – 46 are believed to be allowable at least because of their dependency on claim 24. Claims 48 – 52, 54 – 62 and 64 – 69 are believed to be allowable at least because of their dependency on claim 47.

Claims 2, 25 and 48, as amended, further distinguish over the cited references by reciting that at least one of the processing modules is a sample rate converter module that converts digital audio data between two of the different sampling rates. Claims 2, 25 and 48 further recite that a differing number of the time-slots is used to communicate the digital audio data at the different sampling rates. None of the cited references disclose the conversion of audio data between sampling rates and the communication of audio data at the different sampling rates with a differing number of time-slots.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 480-659-3314 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date May 05, 2008

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 5th day of May 2008.

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